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Cobalt phthalocyanine-based submicrometric field-effect transistors

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We present performance characteristics of nanoscaled cobalt phthalocyanine (CoPc)-based organic field-effect transistors (OFETs) as a function of channel length. We found a channel length range which maximizes the field effect mobility in a trade-off between the decrease in the number of organic grain boundaries and the increase of the electrode–organic contact region. Further reduction of channel length is limited by fringe currents, which lead to an increased off current and to a degradation of the sub-threshold slope. From this, we define an optimal channel length of 280 nm to 1 μm for applications in submicrometric CoPc-based OFETs. Our results are particularly relevant for the miniaturization of chemical sensing OFETs, where metal phthalocyanines have proven to be excellent candidates for the fabrication of the transistor channel.

1 Introduction Metal phthalocyanines (MPc) have high chemical and thermal stability as well as interesting semiconducting properties, which make them excellent candidates for organic field effect transistors (OFETs) [1–6]. In addition, the strong charge transport dependence on the chemical environment makes them also good candidates for chemical sensing. However, in order for MPc devices to be technologically relevant, they need to be miniaturized below the micrometer scale [7, 8]. Indeed, in the current literature there is a wealth of results regarding the miniaturization of OFETs down to the 100-nm regime (see [9] and references therein). The interest in the field is notorious since downscaling MPc-based OFETs would allow for increased circuit density and switching speed [10], while at the same time would decrease the negative effects due to grain boundaries and defects [11–13].

OFET miniaturization is hampered by two important problems. First, transport in devices with small active areas (sub-μm^2) is often dominated by the contact resistance at the electrode/organic layer interface [14–16]. Second, shortening the active channel increases the longitudinal electric field strength, which can lead to fringe currents [17–20]. To account for the fringing currents, corrections need to be applied in the determination of the field-effect mobility, the intrinsic channel conductivity, and the on/off ratio [21].

Here, we report on the fabrication of sub-μm^2 cobalt phthalocyanine (CoPc)-based OFETs and the study of their carrier transport properties as a function of channel length. We chose CoPc (Fig. 1a) for its interesting chemical sensing properties, including an outstanding capability for the detection of low-hazard organic peroxide stimulants used in explosives [22]. We find that, while both the electrode–organic interface and the grain boundaries influence the field-effect mobility, at the smallest channel lengths large longitudinal electric fields result in increased off-current and sub-threshold slope. This analysis reveals an optimal channel length range for sub-μm^2 CoPc-based OFETs. Our study of the electrical response of CoPc-based OFETs in the submicrometer channel length regime might play a fundamental role in the development of smaller sensors.

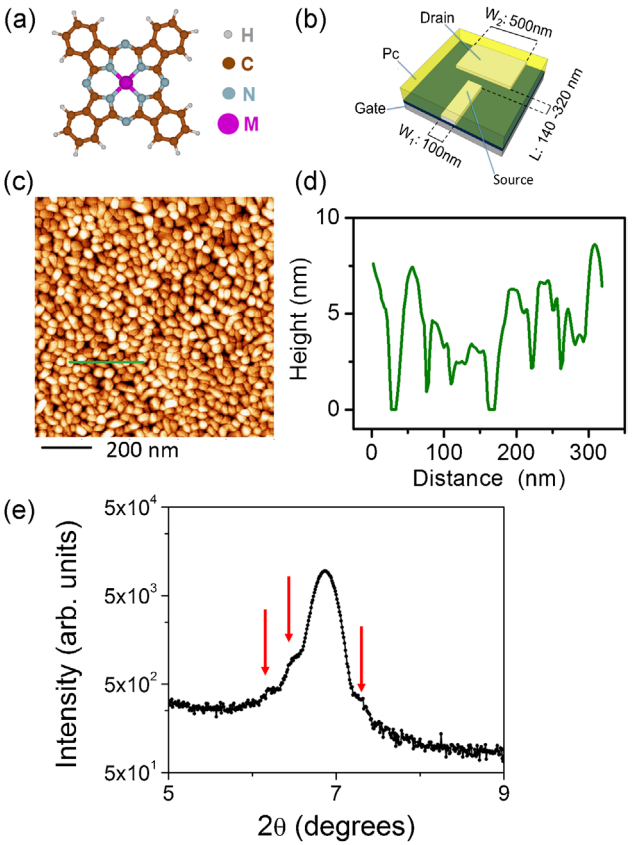

Figure 1 (a) CoPc molecule. H, C, N, and M denotes hydrogen, carbon, nitrogen, and the metallic (Co) atom position, respectively. (b) Schematic nanometric OFET showing the nominal dimensions defined by e-beam lithography: channel length (L) and widths of the source (W_1) and drain (W_2) electrodes. (c) AFM height image of 40-nm-thick CoPc film deposited on SiO_2 substrate. (d) Height profile measured along the green line marked in (c). (e) XRD spectra of 40-nm-thick CoPc film deposited on SiO_2 substrate. The diffraction peak at 6.9° indicates that the CoPc plane forms approximately 65° with the substrate surface and stacks in a chevron structure. Finite size effect peaks (red arrows) indicate high degree of thickness uniformity.

2 Experimental details OFETs were prepared in the bottom-gate bottom-contacts configuration (Fig. 1b). All devices were fabricated on the same chip, consisting of a 150-nm-thick SiO_2 thermally grown on a highly doped p^{++}-type Si substrate. The Si substrate acts as a back gate electrode with the SiO_2 layer being the gate dielectric. Metal electrodes were fabricated using e-beam lithography followed by sputter deposition of 20 nm of Pd and lift-off. Channel lengths (L) were varied from 140 to 320 nm, while channel widths were kept constant for the drain ($W_1 = 100$ nm) and for the source ($W_2 = 500$ nm). The dimensions of the devices were checked by scanning electron microscopy. Different widths of the electrodes were used for making our transistors geometry as general as possible. In the same chip, we also fabricated a standard interdigitated transistor with $L = 1\,\mu$m as a reference for the submicrometric OFETs.

No gate primer or functionalization of the channel or the electrodes were used prior to the CoPc deposition. A 40-nm-thick CoPc film was deposited in all devices on the chip by organic molecular beam deposition (OMBD) at a rate of 0.5 Å s^{-1}, a base pressure of 1.3×10^{-10} mbar, and a substrate temperature of 295 K. Film morphology was examined by atomic force microscopy (AFM) in a sample grown under the same conditions. We found that the film is polycrystalline (Fig. 1c and d) with a typical grain size of 50 nm and a root mean square roughness of 5 nm. X-ray diffraction (XRD) measurement (Fig. 1e) shows a peak at $2\theta = 6.9°$, indicating that CoPc molecules are tilted 65° with respect to the substrate plane and are stacked in a chevron structure [23, 24]. The satellites about the central diffraction peak (red arrows) are finite size effects, and indicate a high degree of thickness uniformity [25].

Electrical measurements were performed in a LakeShore probe station under vacuum (10^{-5} mbar) and in darkness. A Keithley 4200 Semiconductor Characterization System with two source-measure units (SMU) with sub-femto-ampere preamplifiers was used to supply the gate voltage (V_{GS}) and the drain–source voltage (V_{DS}) while (I_{DS}) was being measured. The gate–source current (I_{GS}) was continuously monitored to ensure no significant gate leakage.

3 Results and discussion A typical transfer curve (I_{DS} as a function of V_{GS} for a given drain–source voltage, $V_{DS} = 13$ V) is shown in Fig. 2a. The transfer curves are used to extract the field-effect mobility ($k_{FF}\mu_{FET}$, see below), the threshold voltage (V_{th}), the on/off ratio (I_{ON}/I_{OFF}), and the subthreshold slope (S). However, the unconventional geometry of these devices requires particular procedures as discussed in Ref. [21]. The field-effect mobility is computed as $k_{FF}\mu_{FET} = (L/W_1 C_i V_{DS})(dI_{DS}/dV_{GS})$, where dI_{DS}/dV_{GS} is the slope of the dashed line in Fig. 2a, C_i is the gate insulator capacitance per unit area, and k_{FF} is a dimensionless form factor that takes into account geometry-specific fringe currents. Yet, the field effect mobility extracted in this way is not directly comparable with literature values because here we measure the transfer characteristics at much higher transverse electric field [21]. This further correction will be discussed below. The threshold voltage (Fig. 3a) is computed as $V_{th} = V_0 - V_{DS}/2$, where V_0 is the intercept of the dashed line in Fig. 2a [17]. The on/off ratio, I_{ON}/I_{OFF} (Fig. 3b), is calculated by taking I_{OFF} to be the drain–source current at $V_{GS} = 10$ V, and I_{ON} at $V_{GS} = -30$ V. The subthreshold slope (Fig. 3c) is $S = [d(\log(I_{DS}))/dV_{GS}]^{-1}$. All parameters obtained from the transfer characteristics correspond to the linear and subthreshold regimes.

Typical output characteristics (I_{DS} as a function of V_{DS} for different gate voltages) are shown in Fig. 2b. A clear saturation at high V_{DS} confirms that the transistor is not operating in the short channel regime [26, 27]. The nonlinearity found at low V_{DS} indicates the presence of injection problems due to the formation of a barrier at the electrode–organic interfaces [28].

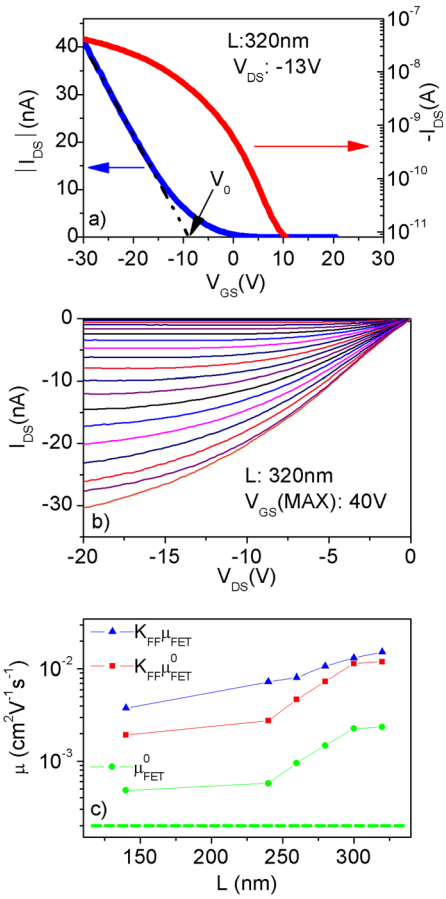

Figure 2 (a) Transfer characteristics (i.e., I_{DS} as a function of V_{GS}) at a drain–source voltage $V_{DS} = -1$ V for the device with $L = 320$ nm. I_{DS} is plotted both in a linear scale (blue line) and in a logarithmic scale (red line). The threshold voltage (V_{th}) and the uncorrected field-effect mobility ($k_{FF}\mu_{FET}$) can be extracted from the former (dotted straight line), whereas the on-off ratio (I_{ON}/I_{OFF}) and the subthreshold slope (S) can be obtained from the latter, as described in the text. (b) Output characteristics (i.e., I_{DS} as a function of V_{DS}) represented for different V_{GS} from 0 to 40 V, in 2 V step, for the device with $L = 320$ nm. (c) Zero-field mobility (μ^0_{FET}) as a function of the OFET channel length. For comparison, the uncorrected field-effect mobility ($k_{FF}\mu_{FET}$) at $V_{DS} = -5$ V and the uncorrected zero-field mobility ($k_{FF}\mu^0_{FET}$) are also plotted. The value obtained from interdigitated transistors with $L = 1$ μm is indicated by the dashed line.

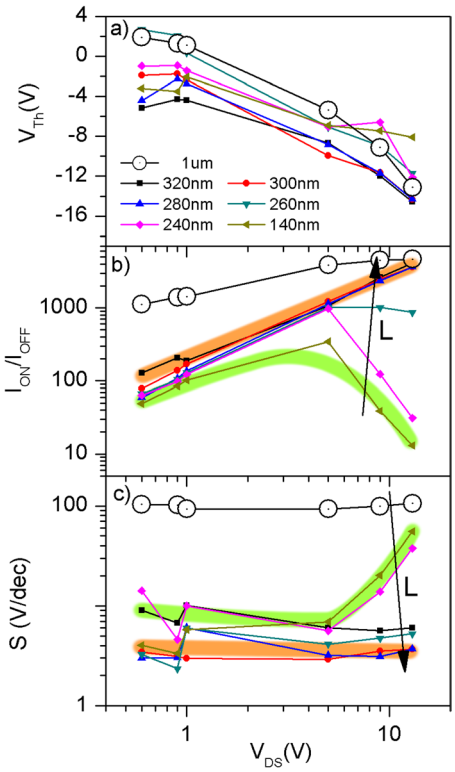

Figure 3 (a) Threshold voltage, (b) on/off ratio, and (c) sub-threshold slope measured as a function V_{DS} and plotted in a logarithmic scale, for OFETs with different channel lengths L. Two different regimes depending on the channel length and V_{DS} value in the on/off ratio and the sub-threshold slope are highlighted with continuous (green or orange) stripes as a guide to the eye. For comparison, the values obtained from an interdigitated transistor with $L = 1$ μm are shown with open circles.

Dependence of $k_{FF}\mu_{FET}$, $k_{FF}\mu^0_{FET}$, and the zero-field mobility (μ^0_{FET}) on L are shown in Fig. 2c. $k_{FF}\mu^0_{FET}$ is computed from $k_{FF}\mu_{FET}$ using the Frenkel–Poole equation $k_{FF}\mu^0_{FET} = k_{FF}\mu_{FET}\exp(-\beta\sqrt{V_{DS}/L})$, where β is the temperature-corrected field-dependent coefficient. The actual zero-field mobility (μ^0_{FET}) is then extracted from $k_{FF}\mu^0_{FET}$ by computing the value of k_{FF} for the specific device geometry [21]. The so corrected μ^0_{FET} values can be now compared with literature values for standard OFETs.

The zero-field mobility peaks for channel length $L = 320$ nm at $\mu^0_{FET} \sim 10^{-3}$ cm^2 V^{-1} s^{-1} (Fig. 2c). For longer channels (interdigitated geometry, $L = 1$ μm, shown as a dashed line in Fig. 2c), the obtained value is $\mu^0_{FET} \sim 2 \times 10^{-4}$ cm^2 V^{-1} s^{-1}, which is in agreement with literature values for CoPc [29]. The lower μ^0_{FET} in longer channels is due to an increase in grain boundaries, which limits the charge transport in polycrystalline thin films [30]. μ^0_{FET} also decreases for very short channels (5×10^{-4} cm^2 V^{-1} s^{-1} for $L = 140$ nm), because the contact resistance becomes larger than the channel resistance when the channel length is comparable to (or smaller than) the size of the contact region [14, 31]. A similar trade-off between the negative effect of grain boundaries and the relative contact resistance has been observed in pentacene-based OFETs [21].

The dependence of V_{th}, I_{ON}/I_{OFF} ratio and S on V_{DS} and L is summarized in Fig. 3. Reference data obtained for the interdigitated transistor is also included for comparison. Figure 3a shows V_{th} as a function of V_{DS} for different L devices. In an ideal transistor, V_{th} should not change with L or V_{DS} [32]. However, in these devices, V_{th} decreases with increasing V_{DS}. This behavior is known as "bias stress". This stress due to V_{GS} bias is induced by the measurement sequence since every increase in V_{DS} in the plot was

performed after a complete V_{GS} sweep [33]. Indeed, bias stress manifests as a continuous shift of V_{th} upon prolonged or repetitive application of gate bias [34]. On the other hand, the dispersion of V_{th} for different L for a fixed V_{DS} indicates the presence of trapped charges in the gate–dielectric interface [35].

Figure 3b shows the I_{ON}/I_{OFF} ratio as a function of V_{DS} for different L. As mentioned, it is computed as the ratio between the I_{DS} at $V_{GS} = -30$ V and the I_{DS} at $V_{GS} = 10$ V. Figure 2a shows that outside those values I_{DS} does not change significantly, but might produce a breakdown of the gate dielectrics. This measurement is limited by the noise level of the source-meter (10^{-11} A), which determines the cut-off for the off state. Above 280 nm, the I_{ON}/I_{OFF} ratio increases linearly with V_{DS}. This is because the measured I_{OFF} value is limited by the source-meter resolution while the I_{ON} value increases linearly with channel bias. Although in an ideal case the I_{ON}/I_{OFF} ratio is not expected to vary with L [36], a clear decrease in the on/off ratio appears for small L ($\leq$260 nm) above 5 V. This reduction is caused by the increase of the I_{OFF} value (above 10^{-11} A) due to a parallel ohmic current flowing through the bulk of the CoPc channel that becomes relevant at a large enough longitudinal electric field (associated with a high V_{DS} and a small L) [36].

Sub-threshold slope S as a function of V_{DS} at different L is presented on Fig. 3c. This parameter is not expected to vary with either V_{DS} or L [37]. For $L > 250$ nm, the observed variation of S with L is due to the device-to-device trap density variation at the interface of the gate-dielectric layer [38]. This further confirms uncontrolled presence of trapped charges at the gate dielectric interface. However, for the smallest channels ($L \leq 240$ nm) and the highest applied fields ($V_{DS} \geq 5$ V) there is an increase in S indicating a clear degradation of the transistor performance. This behavior is related to the degradation observed in Fig. 3b caused by parallel ohmic currents, which results in a shift in the drain current and, consequently, the appearance of a long tail in the semi-log plot at the subthreshold region. Such an effect would lead to a more gradual onset of conduction, which would mainly affect transistor parameters extracted from the off regime (the I_{ON}/I_{OFF} ratio and S) and not from the on regime (μ^0_{FET} and V_{th}).

Finally, an optimal operational region for the performance of these devices can be defined based on the combination of all of the aforementioned effects. As a general rule, for transistors operating in the linear regime, it is useful to operate them at the maximum available V_{DS} and the smallest possible L. As evident from Fig. 3, there is a trade-off between reduction of L below 260 nm and an increase in the absolute value of V_{DS} above 5 V. This is an important limiting factor in the future use of MPc-based OFETs in applications where a high-density array of devices or high-operating voltages are needed. However, the results hold promise for OFET sensing applications where restrictions on channel lengths are not as stringent. At present it is not clear whether the deviations from ideality are related to the thin film growth or lithography and therefore further studies of nanopatterned arrays of sensors is needed [1–3].

4 Conclusions In conclusion, we have studied the behavior of nanoscaled OFETs based on CoPc. We observe a clear improvement in the transport properties (field-effect mobility) with respect to their micrometer-sized counterparts. This is attributed to a decrease in the number of grain boundaries between electrodes. However, when the channel length is decreased below 320 nm and the length becomes comparable to (or smaller than) the extension of the contact region, the field-effect mobility decreases. This behavior is attributed to the contact resistance, which dominates the device transport at the smallest channel lengths. In addition, the large longitudinal electric fields at the smallest channel lengths cause fringing currents, which lead to an increased off current and to the degradation of the sub-threshold slope. These limitations define an optimal channel length of 280 nm to 1 μm for the applications of submicrometric CoPc-based OFETs, including chemical vapor sensing.

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